IN THE FIGURES

A replacement sheet is included for Figure 1. In this replacement sheet, Figure 1 has been amended to include the legend "-- Prior Art --" as requested by the Examiner.

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REMARKS

Applicant gratefully acknowledges the indication that claims 1, 9 - 15, and 17 - 20 recite allowable subject matter.

However, Applicant respectfully traverses the rejections of the remaining claims as being obvious over Applicant's Figure 1 in view of the Hadidi reference (USP 5,489,904). For example, consider claim 1, which recites a subranging ADC having both a first and a second integrating sample-and-hold circuit. In contrast, the conventional sub-ranging ADC of Applicant's Figure 1 has just a single voltage-tracking (not integrating) sample-and-hold circuit. Applicant has highlighted the word "integrating" as the advantages of using an integrating sample-and-hold circuit (as opposed to the conventional voltage-tracking sample-and-hold circuit of Figure 1) were noted on page 6, lines 10 - 16. For example, by using an integrating sample-and-hold circuit, the need for feedback control of the switch is eliminated.

The Hadidi reference has been cited for its use of "two sets of differential pairs." As set forth in Hadidi's abstract, "the transconductance of one differential pair is scaled relative to the transconductance of the other differential pair." This leads to the core of Hadidi's

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disclosure: "As a consequence, the same resistor string may be used for two different digital-to-analog converters of the subranging circuit." This consequence may be better understood with reference to Hadidi's Figure 2 and 3. The digital-to-analog (DAC) of Hadidi's Figure 2 (element 42) has precisely the same function as the DAC in Applicant's Figure 1. All that Hadidi recognized was a way to make this DAC operate faster by splitting it into two DACs (elements 50 and 58) as seen in Hadidi's Figure 3. But note that a digital-to-analog converter is merely converting a digital word into an analog value: because the DAC is presented with a digital word, it needs absolutely no association with sample-and-hold circuit (regardless of whether the sample-and-hold circuit is an integrating or voltage-tracking type).

Accordingly, there can be no teaching or suggestion from Hadidi's two DAC approach to modify Applicant's Figure 1 to have two sample-and-hold circuits, let alone the two integrating sample-and-hold circuits as recited in claim 1. Furthermore, there is no teaching or suggestion from either Hadidi or Applicant's Figure 1 to provide a "a second stage configured to receive charge from the charged second capacitor and the analog voltage to provide a voltage difference between the sampled input voltage and the analog

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voltage, the second stage including a fine-quantizing ADC configured to convert the voltage difference to provide a finely-digitized output." This is a patentable distinction because as pointed out by the Applicant on page 7, lines 5 - 7, rather "than use an amplifier to indirectly determine the difference between $V_{sample1}$ and coarse sample voltage 220, subranging ADC 200 performs this operation directly by transferring the charge accumulated on capacitor C1 [the capacitor in the second integrating sample-and-hold circuit]." In glaring contrast, as seen for in Figures 2 and 3, Hadidi uses an amplifier (elements 46 and 66) as is the case for Applicant's Figure 1. Thus, Hadidi requires the circuitry and resulting power consumption of an amplifier whereas Applicant's claimed ADC eliminates this component.

Accordingly, claim 1 and its dependent claims 2 - 13 are plainly patentable over the combination of Applicant's Figure 1 and the Hadidi reference. Claim 14 is a method claim that is patentable over the cited prior art analogously as discussed with respect to claim 1 - see, e.g., the transferring charge act recited in claim 14. Because claim 15 depends upon claim 14, it is allowable for at least the same reasons. Claim 15 and its dependent claims 16 - 20 recite a first integrating sample-and-hold

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circuit "configured to sample an input voltage by charging a first capacitor" and a "means for determining a residual voltage equaling the difference between the analog voltage and the voltage on the charged first capacitor" and are thus also patentable over the cited prior art.

A replacement sheet is provided for Figure 1 that includes the legend "Prior Art."

Claim 17 has also been amended to address the informality noted by the Examiner.

If there are any questions regarding any aspect of the application, please call the undersigned at (949) 752-7040.

Certification of Facsimile Transmission
I hereby certify that this paper is being facsimile transmitted to the U.S. Patent and Trademark Office on the date shown below.

Saundra Carr August 9, 2005
Saundra Carr Date of Signature

Respectfully submitted,

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